What Is Claimed Is:

1. An optical communications apparatus, comprising:

an optical bench comprising a substrate having an electrical turning via formed therein;

an optoelectronic (OE) chip; and

an integrated circuit (IC) chip,

wherein the OE chip and IC chip are mounted on the optical bench and electrically connected using the electrical turning via.

2. The apparatus of claim 1, wherein the OE chip comprises a vertical-cavity surface-emitting laser bar (VCSEL).

3. The apparatus of claim 1, wherein the IC chip comprises a laser driver.

4. The apparatus of claim 1, wherein the OE chip comprises a photodetector array.

5. The apparatus of claim 1, wherein the IC chip comprises an amplifier.

6. The apparatus of claim 1, wherein the apparatus comprises an OE receiver package, an OE transmitter package, or an OE transceiver package.

7. The apparatus of claim 1, wherein the substrate comprises a silicon substrate.

8. The apparatus of claim 1, further comprising an optical transmission line mounted or formed on the optical bench.

9. The apparatus of claim 8, wherein the OE chip and optical transmission line are disposed on the optical bench such that a center axis of the optical transmission line is substantially perpendicular to a light-emitting or light receiving surface of the OE chip.

10. The apparatus of claim 8, wherein the optical bench comprises an alignment mark etched in the substrate for aligning the OE chip to the optical transmission line.

11. The apparatus of claim 10, wherein the OE chip comprises an alignment mark that matches the etched alignment mark in the substrate.

12. The apparatus of claim, 8 wherein the optical transmission line comprises an optical fiber mounted on the optical bench.

13. The apparatus of claim 8, wherein the optical transmission line comprises a waveguide structure formed on a surface of the substrate.

14. The apparatus of claim 1, wherein the optical bench further comprises a v-groove channel etched in the substrate for mounting an optical fiber, and an alignment mark that is co-etched with the v-groove channel.

15. The apparatus of claim 1, wherein the OE chip comprises a ledge structure on a surface thereof for providing push-stop alignment when mounted on the optical bench.

16. The apparatus of claim 15, wherein the optical bench further comprises an etched cavity for mountably receiving the OE chip, the etched cavity comprising a step structure that contacts the ledge structure of the OE chip.

17. The apparatus of claim 1, wherein the electrical turning via is terminated with solder bumps.

18. The apparatus of claim 1, wherein the electrical turning via comprises at least one 90 degree bend.

19. The apparatus of claim 1, wherein the electrical turning via has a first end portion exposed on a first surface of the substrate and a second end portion exposed on a second surface of the substrate, the first and second surfaces defining planes that are substantially perpendicular.

20. The apparatus of claim 1, wherein the OE chip and IC chip are mounted on the optical bench such that a light-emitting or light-detecting surface of the OE chip is substantially perpendicular to a surface of the IC chip having contacts.

21. An optical bench, comprising:

a substrate having a first surface, a second surface and a third surface, wherein the first and second surfaces define planes that are substantially parallel, and wherein the third surface defines a plane that is substantially perpendicular to the planes defined by the first and second surfaces; and

a conductive via formed in the substrate, the conductive via having a first end portion exposed on the

third surface, and a second end portion exposed on the second surface.

22. The optical bench of claim 21, further comprising a first insulation layer formed on the first surface and a second insulation layer formed on the second surface, wherein the second insulation layer has an opening to the second end portion of the conductive via exposed on the second surface.

23. The optical bench of claim 21, wherein optical bench comprises a cavity having a sidewall defined by the third surface.

24. The optical bench of claim 23, wherein the cavity sidewall and first surface define an edge.

25. The optical bench of claim 24, wherein the edge is used for push-stop alignment of an OE chip when the OE chip is mounted to the optical bench.

26. The optical bench of claim 23, wherein alignment marks are formed on the optical bench near the edge.

27. The optical bench of claim 23, wherein the cavity sidewall is used for push-stop alignment of an OE chip, when the OE chip is mounted on the optical bench.

28. The optical bench of claim 21, further comprising a v-groove channel etched in the first surface and a corresponding co-etched alignment mark.

29. The optical bench of claim 21, further comprising a waveguide structure formed on the first surface.

30. The optical bench of claim 21, wherein the optical bench is structured for packaging a optoelectronic transmitter, an optoelectronic receiver or an optoelectronic transceiver.

31. A method for fabricating an optical bench, comprising the steps of:

providing a substrate having a first surface and a second surface, the first and second surfaces defining planes that are substantially parallel;

etching a via hole through the substrate between the first and second surfaces;

etching a first cavity in the first surface, wherein the first cavity overlaps a first end portion of the via hole exposed on the first surface;

filling the via hole and first cavity with a conductor to form a conductive via.

32. The method of claim 31, further comprising etching a second cavity in the second surface, wherein the second cavity overlaps a second end portion of the via hole exposed on the second surface, and filling the second cavity with the conductor.

33. The method of claim 31, further comprising etching a cavity in the substrate below the first surface to expose a portion of the conductor in the first cavity on a sidewall of the cavity, the sidewall of the cavity being substantially perpendicular to the first and second surfaces.

34. The method of claim 33, further comprising forming a solder bump on the exposed portion of the conductor of the first cavity.

35. The method of claim 31, further comprising:

forming an insulating layer on the first and second surfaces of the substrate;

forming an opening the insulating layer on the second surface to expose a second end portion of the conductive via on the second surface of the substrate; and

forming solder bump on the exposed second end portion of the conductive via.

36. The method of claim 31, further comprising:

etching a v-groove in the first surface of the substrate for hosting an optical fiber; and

etching an alignment mark in the first surface of the substrate to correspond to the etched v-groove.